THAT WHICH IS CLAIMED IS:

1. A method for stabilizing the voltage on the drain terminals of multi-level non-volatile memory cells in the programming step, of the type wherein the application of said voltage is provided through a drain voltage regulator having an output connected to said terminals in a common circuit node by a metal line conduction path having a parasitic intrinsic resistance, characterized in that it is provided with a feedback path between said node and an input of the regulator.

2. A method according to claim 1, characterized in that said feedback path comprises a resistance and a parasitic intrinsic resistance having a negligible value.

3. A method according to claim 1, characterized in that said input of the regulator is the inverting input.

4. A method according to claim 1, characterized in that it is provided with a buffer inserted between said output of the regulator and said node, as well as a feedback path between said node and an input of said buffer.

5. A method for stabilizing the voltage at both ends of a load among a plurality of loads associated to a supply line and active one at a time, of the type in which the application of said voltage is

provided by a voltage regulator having an output connected to the loads through said supply line and a plurality of routing resistances each one being associated with a corresponding load, characterized in that it provides a feedback path between one end of the farthest load from the regulator and an input of the regulator itself.

6. A method according to claim 5, characterized in that said feedback path comprises only a parasitic intrinsic resistance having a negligible value.

7. A multi-level non-volatile memory electronic device monolithically integrated on a semiconductor and comprising a programming circuit associated with a matrix of non-volatile memory cells, each one being equipped with at least a floating gate transistor with corresponding source, drain and gate terminals, each programming circuit incorporating a drain voltage regulator having an output connected to the cell drain terminals in a common circuit node and through a metal line conduction path having a parasitic intrinsic resistance, characterized in that it comprises a feedback path between said node and an input of the regulator.

8. A device according to claim 6, characterized in that said feedback path comprises a resistance and a parasitic intrinsic resistance having a negligible value.

9. A device according to claim 6, characterized in that said input of the regulator is the inverting input.

10. A device according to claim 6, characterized in that it provides a buffer inserted between said output of the regulator and said node, as well as a feedback path between said node and an input of said buffer.